

U.S. Serial No. 09/414,226  
Chang 7-20-10

IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Chorng-Ping Chang  
Chien-Shing Pai  
Thi-Hong-Ha Vuong

Case: 7-20-10

Serial No.: 09/414,226

Group Art Unit: 2811

Filing Date: October 7, 1999

Examiner: Donghee Kang

Title: Semiconductor Device with Tapered Gate and Process For  
Fabricating the Device

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ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231

AUG 9 2002

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SIR:

**AMENDMENT AFTER FINAL AND REQUEST FOR RECONSIDERATION**  
**PURSUANT TO 37 C.F.R. § 1.111**

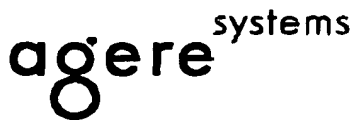
This reply is in response to the Official Action mailed June 15, 2001.

**IN THE CLAIMS**

1. (twice amended) A semiconductor device comprising:  
a semiconductor substrate in which a source, drain and channel are  
formed;  
a gate formed on a gate dielectric layer formed on the semiconductor  
substrate;  
spacers adjacent to the gate wherein the gate is interposed between the  
spacers the gate and spacers are formed in a trench formed in a layer of

#10/C  
8-13-02  
Payton  
(NE)

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## FAX COVER SHEET

Date: August 9, 2002	No. of pages: 7 (including cover)
To: Donghee Kang	From: Richard J. Botos
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Serial No. 09/414,226; C.P. Chang 7-20-10

Transmittal Letter (1 page)  
Amendment After Final (5 pages)

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IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Chorng-Ping Chang  
Chien-Shing Pai  
Thi-Hong-Ha Vuong

CASE 7-20-10

Serial No. 09/414226 Group Art Unit 2811

Filed October 7, 1999

Examiner D. Kang

Title Semiconductor Device With Tapered Gate And Process For Fabricating The Device

ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231


SIR:

Enclosed is an amendment in the above-identified application.

NO ADDITIONAL FEE REQUIRED

In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 501735** as required to correct the error.

Respectfully,

  
Richard J. Botos, Attorney  
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908-582-3809.

Date: 8/09/02

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